

Influence of Reflow Profile and Pb-Free Solder Paste in Minimizing Voids for Quad-Flat Pack No-Lead (QFN) Assembly

Authored by: Tim Jensen and Ed Briggs, Indium Corporation, Harish Gadepalli, Rangaraj Dhanasekaran, and Dr. S. Manian Ramkumar.

Abstract

Quad-Flat Pack No-lead (QFN) packages have become a popular choice in electronics packaging due to their small form factor. They are also gaining rapid industry acceptance because of its excellent thermal and electrical performance. The bottom side of the QFN package has a large thermal pad. This exposed die-attach pad effectively conducts heat to the PCB and also provides a stable ground connection. Effective soldering of this surface to the pad on the PCB is required for good thermal dissipation and component functionality. The exposed thermal pad presents various challenges during the surface mount assembly process. One major challenge is solder void formation. Voids are primarily formed due to the entrapment of volatiles in flux outgassing during the reflow process.

The primary objective of this study is to determine optimal parameters to minimize void formation in QFN packages (QFN16 and QFN20), specifically the reflow profile, lead-free solder paste and stencil aperture opening for the thermal pad. A systematic DOE based approach was used to arrive at conclusions, using the ratio of void volume on the thermal pad to the actual volume of solder paste printed as the response variable. Various graphs are presented to understand the impact of different parameters. Interaction graphs were used to determine optimal settings for each parameter.

Introduction

QFN, which is also referred to as MicroLeadFrame® (MLF), is a near CSP plastic encapsulated leadless package with a copper lead frame substrate. Unlike the traditional packages, where the leaded terminations are soldered to the PCBs, the electrical contacts in QFNs are achieved by soldering the leads on the bottom surface of the package to their corresponding pads on the PCB. The unique construction of this package also incorporates a large heat-sinking pad in the middle of the package on the bottom. This efficiently conducts

the heat away from the component. The bond wires and the down bonds provide electrical and ground connections (Figure 1).

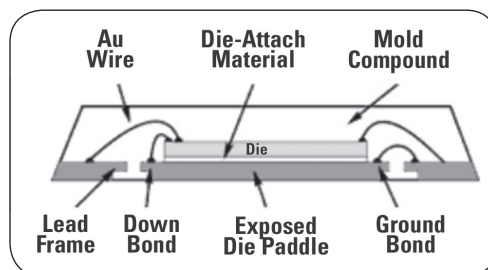


Figure 1. QFN package construction.

TIM JENSEN



Tim Jensen, Product Manager for Engineered Solders Materials, is an SMTA-certified process engineer. He has more than 15 years of experience working with customers troubleshooting and optimizing SMT process lines and solving defects, such as head-in-pillow, graping, and QFN voiding.

Tim has worked directly on hundreds of surface mount lines and developed a number of different products. Using that direct knowledge and expertise, he works closely with Indium Corporation's technical service, sales, and research and development teams to develop cutting-edge products that address the unique challenges faced by the electronics assembly industry. As senior product manager, Tim is responsible for Indium Corporation's most diverse product group, which includes solder preforms, wire, ribbon and foil, as well as thermal interface materials. He earned his bachelor's degree in chemical engineering from Clarkson University and his master's in business administration from Syracuse University.

email: tjensen@indium.com

Full biography:
www.indium.com/biographies

QFN packages provide a great amount of flexibility from the design standpoint. With few design changes, the operating frequencies can be increased up to 10GHz [1]. The small form factor coupled with excellent electrical and thermal performance makes the QFN package an ideal choice for handheld products and miniaturized electronic applications.

Assembly Issues

One of the major challenges during QFN assembly is minimizing voids in the solder joint of the thermal pad. However, eliminating voids completely is impossible because of the presence of thermal vias and the large size of the thermal pad. Voids are formed due to the outgassing of volatiles during the reflow process and its entrapment in the solder joint. When the solder paste is heated to liquidus, the gases created by the volatilized compounds must exit the molten solder mass. This is more prevalent in the thermal pad area because of the higher volumes of paste. The presence of voids will affect the performance of the component and eventually lead to premature failure.

High Centering

Normally, in the lead-free assembly process, the aperture opening to pad ratio in the PCB is 1:1. The difference in size between the large thermal pad and the small I/O pads of the QFN presents a challenge in producing an even solder-line thickness. Since the opening for the center aperture in the stencil is too large, the solder paste deposits in the center will be taller than the deposits on the I/O terminals. In this case, the paste on the thermal pad lifts the component up and the I/O terminations never get an opportunity to come in contact with the pads on the PCB (Figure 2).



Figure 2. High centering due to excess solder in the PCB thermal pad area.

From a reliability perspective, the signal pads should have a standoff height of at least 50–75µm after assembly [1]. On the other hand, due to the presence of a single large aperture opening in the stencil, the squeegee might deform and scoop away some of the paste. This can lead to uneven paste deposition and hence solder void formation. Several studies in the past have investigated various design and process parameters that can reduce the formation of voids in the thermal pad area. One of the studies suggests that 50–80% of solder paste coverage on the thermal pad area would be desirable to control void formation [2]. The higher the percentage of paste, the greater the probability for the volatiles to get entrapped within the solder joint and hence higher the chances for void formation.

Another study evaluated the impact of different stencil aperture openings on the void formation [3]. This study recommended segmenting the aperture into series of small openings (Figure 3). The authors indicate that, as opposed to one large single opening for the thermal pad area, segmenting would help achieve 50–80% solder paste coverage with even paste deposition.

The paste, which is printed using a modified stencil design, will have adequate spacing to promote effective outgassing of volatiles and hence the possibility for less void formation. Industry investigations suggest that a cumulative void volume within the solder joint, which is less than 50% of the thermal pad area, does not result in thermal or board level performance degradation. The voids which are bigger than the via hole pitch, under the thermal

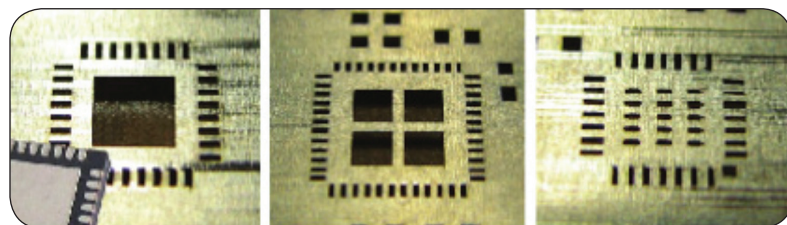


Figure 3. Modified stencil design for thermal pad.

EDWARD BRIGGS



Edward Briggs, Regional Sales Manager – Northeastern United States and Eastern Canada, joined Indium Corporation in 1992 and has held a variety of positions in production and technical support.

Ed is an SMTA-certified engineer, and earned his Green Belt Six Sigma certification from Dartmouth College for demonstrating proficiency in developing and executing design experiments to support continuous process improvement.

Ed has an associate's degree in chemical technology from Mohawk Valley Community College, where he won the Douglas J. Bauer Award for Excellence in Chemistry. He has authored numerous technical papers and has presented at several technical conferences throughout North America.

email: ebriggs@indium.com

Full biography:

www.indium.com/biographies

pad area, might have an adverse effect on high speed and RF applications [1]. From the PCB design standpoint, masking the thermal vias underneath the thermal pad will prevent solder wicking and hence minimize void formation. Parameters, like reflow profile, peak temperature, and the type of solder paste, have a strong influence on void formation. The issue of voiding becomes even more pronounced when QFN assembly is coupled with lead-free solder paste. Lead-free solder alloys form more volatiles at elevated temperatures. The tendency of these volatiles to escape from a lead-free solder is less when compared to the traditional tin-lead (SnPb) solder. Other paste parameters, such as flux content, solvent concentration, boiling temperature, and flux activator concentration play an active role in volatile formation. Modifications to the solder paste flux system can significantly reduce void formation.

Experiment Methodology

A general full factorial experiment was designed for this study. The factors that were used in the experiment and their corresponding levels are listed in Table 1. Each of these factors must be properly controlled to minimize voids. A DOE-based approach was also used to study the effect of each individual variable and their corresponding interactions on the void formation.

Table 1. Factors and levels of the experiment.

Factors	Level 1	Level 2	Level 3
Paste	Indium5.1AT	Indium8.9	-
Finish	OSP	ImAg	-
Profile	Tent with 235°C peak	Tent with 250°C peak	-
Component	QFN16	QFN20	-
Pattern	A	D	E
Percentage	30%	50%	70%

Based on the number of factors and their corresponding levels, a total of 144 runs were used to analyze the experiment. The run orders of the experiment were completely randomized to reduce variability. Three replicates were conducted for each combination because they provide an estimate of the experimental error and the effect itself. The levels for each factor were considered based on experience and literature review. The ratio of void volume to the actual paste volume printed was used as the response variable.

Factors Incorporated in the Experiment

Solder Paste

Indium5.1AT and Indium8.9 Solder Pastes were chosen to provide solder pastes that encompass two major approaches for PCB assembly. Indium8.9 Solder Paste was designed to have a highly probe testable flux residue. There is much concern

in the industry that probe testable solder pastes may suffer some in reflow performance (including voiding). Indium5.1AT Solder Paste has a more traditional hard residue. By testing these two solder pastes, the research study was able to address the main solder paste technology approaches and determine whether there was any validity to the concern that probe test-friendly solder pastes may not reflow as well (and consequently produce more voids).

PCB Finish

OSP and ImAg were two levels that were incorporated for understanding the effect of PCB surface finish. These two finishes are considered viable lead-free alternatives. OSP, being an organic finish, is expected to provide more voids during the reflow process.

Reflow Profile

Two tent reflow profiles with different peak temperatures (Figures 4 and 5) were used in the experiment. The preheat rate and TAL were fixed at 1°C/sec and 60sec, respectively. The actual values that were observed in the reflow oven are included in Table 2.

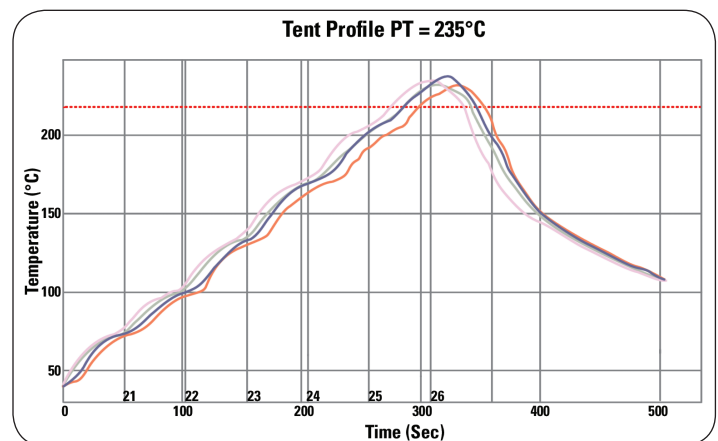


Figure 4. Tent profile with 235°C peak temperature.

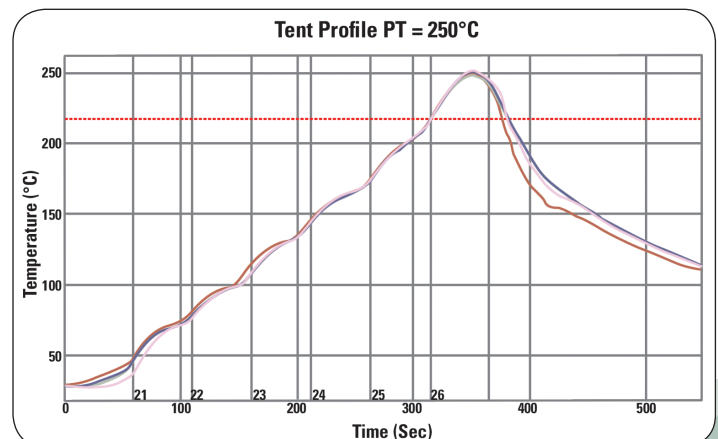


Figure 5. Tent profile with 250°C peak temperature.

Table 2. Observed reflow profile parameters.

Profile	Preheat Rate (°C/sec) 25–217°C	TAL (sec)	Peak Temperature (°C)
Tent-235	0.90–1.22	55–63	231–237
Tent-250	0.94–1.17	62–69	248–252

Component

The two levels for components include QFN16 and QFN20. Both components had the same thermal pad area. The primary difference between the QFN16 and QFN20 is the number of signal pads surrounding the thermal pad area. The component dimensions are presented in Table 3. Figure 6 shows the distinction between the two components. All the components that were used in conducting the experiment had lead-free finish on its terminations (tin).

Table 3. Component dimensions.

Component	Pad Width (mm)	I/O Count	Pitch (mm)	Thermal Pad Area (mm ²)
QFN16	2.94	16	0.8	8.6436
QFN20	2.93	20	0.65	8.5849

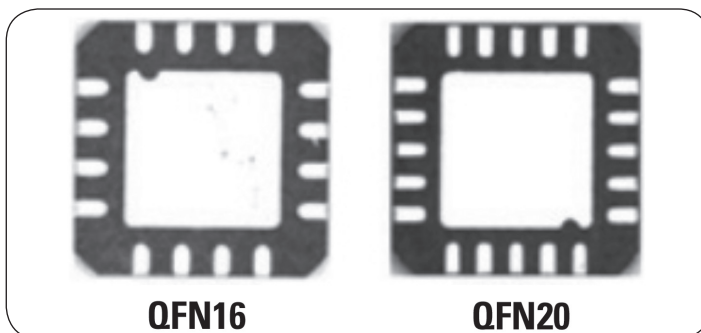


Figure 6. QFN16 and QFN20, bottom view.

Pattern and Percentage of Solder Paste

Three different patterns (A, D, and E) were used to analyze the formation of voids as a function of aperture opening in the stencil.

Three different solder volumes (30, 50, and 70%) were used in the experiment. These different solder volumes were printed using all the patterns to understand the voiding behavior, corresponding to the volume printed. Figure 7 shows the three patterns which were used and the respective size of the print along with separation distance between the apertures and the edge of the thermal pad. Increased volumes of pastes were achieved using apertures with bigger openings. Table 4 lists the dimensions of the apertures and the separation distance.

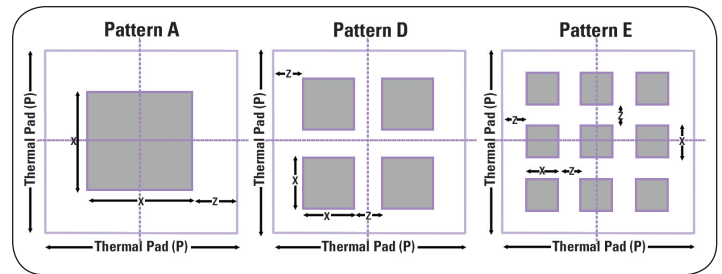


Figure 7. Aperture patterns in the stencil.

Table 4. Aperture size and separation distance (QFN16 and QFN20).

Pattern	Paste %	QFN16		QFN20	
		X (mm)	Z (mm)	X (mm)	Z (mm)
A	30%	1.61	0.67	1.60	0.67
A	50%	2.08	0.43	2.07	0.43
A	70%	2.46	0.24	2.45	0.24
D	30%	0.81	0.44	0.80	0.44
D	50%	1.04	0.29	1.04	0.29
D	70%	1.23	0.16	1.23	0.16
E	30%	0.53	0.34	0.53	0.34
E	50%	0.69	0.22	0.69	0.22
E	70%	0.82	0.12	0.81	0.12

Test Vehicle

Two different test vehicles, one with OSP finish and the other with ImAg finish, were used in the analysis. Both PCBs were a lead-free standard FR-4 substrate. The location of each pattern on the board was completely randomized to minimize the sources of variation. Figure 8 displays the test vehicle that was used in the experiment.

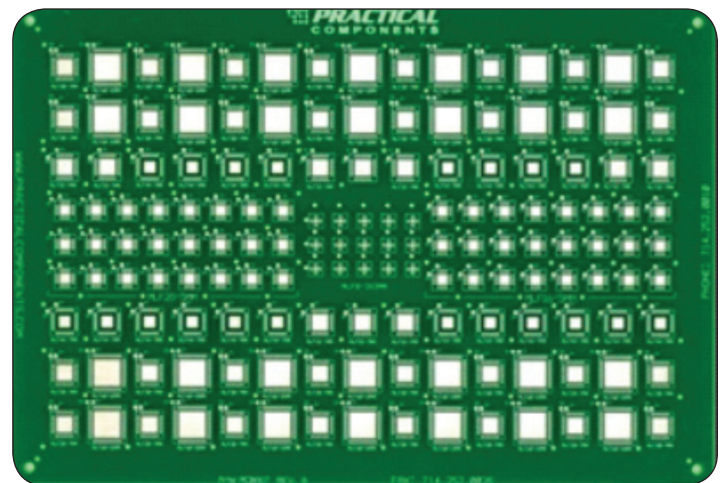


Figure 8. Test vehicle.

Process Steps

1. A 5mil-thick, laser cut stencil was used to print the paste on the test vehicle.
2. The actual paste volume on the thermal pad was measured after every print. The actual volume was compared against the theoretical volume to obtain transfer efficiency. The overall average paste transfer efficiency was 82.74%.
3. Components were assembled using the Siemens pick and place machine, using a placement force of 2N.
4. Based on the experimental runs, the assemblies were subjected to the appropriate reflow profile.
5. A cross sectional study was conducted on 10 randomly selected samples with 30% print, to observe the paste spread after reflow. It was found that even with the minimum paste, the solder had spread over the entire thermal pad area (Figure 9). Also the void was found to fill the entire thickness of the joint, with no taper.

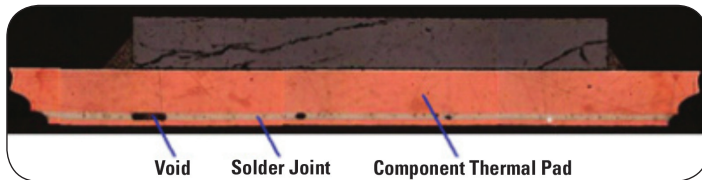


Figure 9. Component cross section.

Data Collection

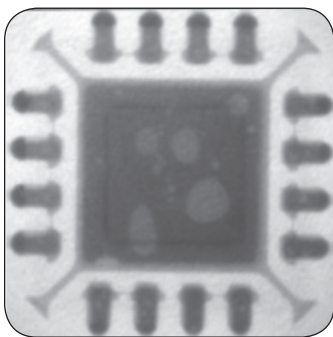


Figure 10. X-ray image of a QFN.

The assembled boards were inspected for voids using the Glenbrook X-ray inspection system. All measurements were taken at the same Z-level, frame size, voltage, current, resolution, brightness, contrast, color, filter, etc. to measure the effective area of void for each type of component. A Gage R&R study was performed on the X-ray inspection system

prior to the void measurement in order to ensure repeatability and reproducibility. Figure 10 shows an X-ray image of a QFN with voids.

Response Variable

The response variable used in the analysis is the ratio of the volume of void (V_{VOID}) to the actual volume of solder paste printed on the thermal pad (V_{ACTUAL}). The parameter V_{VOID} has

to be calculated based upon the area of void (A_{VOID}) measured using the X-ray system. The actual volume of solder paste (V_{ACTUAL}) is measured after the print process and was used in determining the response variable.

$$V_{VOID} = A_{VOID} \times \text{Solder Joint Thickness (T)}$$

$$T = \frac{V_{ACTUAL}}{2 \times (A_{TP} - A_{VOID})}$$

where A_{TP} is the area of the thermal pad and the volume of the solder joint is half the actual volume of solder paste printed on the thermal pad. Therefore,

$$V_{VOID} = \frac{A_{VOID} \times V_{ACTUAL}}{2 \times (A_{TP} - A_{VOID})}$$

$$V_{VOID} = \frac{A_{VOID} \times V_{ACTUAL}}{2 \times A_{TP} \left(1 - \frac{A_{VOID}}{A_{TP}}\right)}$$

Let

$$\text{Void Ratio (X)} = \frac{A_{VOID}}{A_{TP}}$$

Therefore,

$$\text{Response Variable} = \frac{V_{VOID}}{V_{ACTUAL}} = \frac{X}{2(1-X)}$$

Results and Discussions

The response variable obtained for the various runs was checked for normality, using a 95% confidence interval. The normality test revealed that the data is normally distributed (Figure 11). The experiment was further analyzed using the analysis of variance (ANOVA) technique to identify significant factors and interactions.

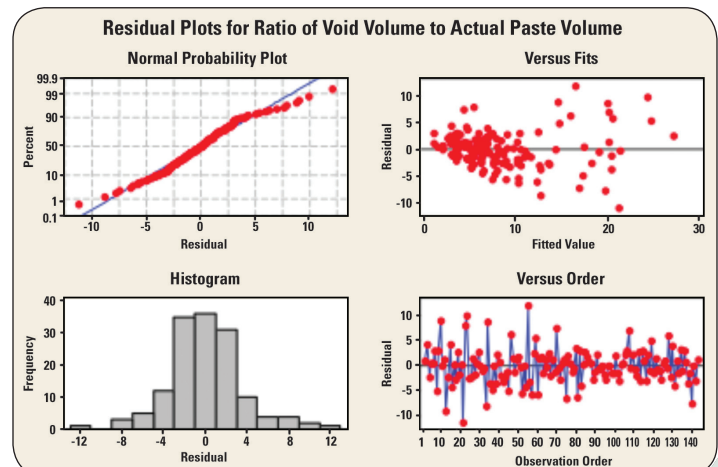


Figure 11. Residual and normal probability plots.

Table 5. List of significant factors and interactions.

Factor(s)	p-Value
Pattern	0.001
Percentage	0.000
Profile	0.000
Pattern * Profile	0.404
Percentage * Profile	0.000
Percentage * Finish	0.024
Profile * Paste	0.005
S = 4.06149	R-Sq = 70.69% R-Sq(adj) = 61.54%

The main effect plots of the factors provide an estimate of the influence of each factor on the formation of voids. Some significant conclusions that could be drawn from the main effect plots (Figures 12 and 13) include:

1. Pattern A provided the least voiding. Void behavior was approximately the same for patterns D and E.
2. As volume increases, the void percentage also increases.
3. Tent profile with 250°C peak temperature performed better under all circumstances.
4. QFN16 provided slightly less voiding when compared to QFN20. This can possibly be attributed to the I/O pitch, which is 150µm lower for QFN20 when compared to QFN16. The higher pitch in QFN20 provides more opportunity for the volatiles to escape and hence provides fewer voids.
5. The effect of paste was less significant.
6. ImAg performed slightly better when compared to OSP.

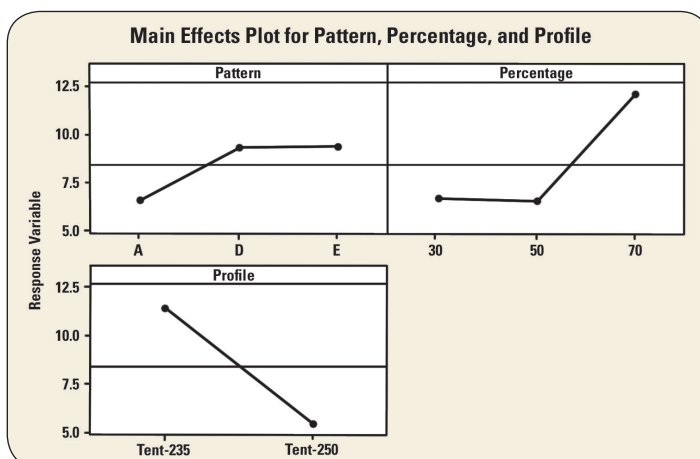


Figure 12. Main effects plot of significant factors.

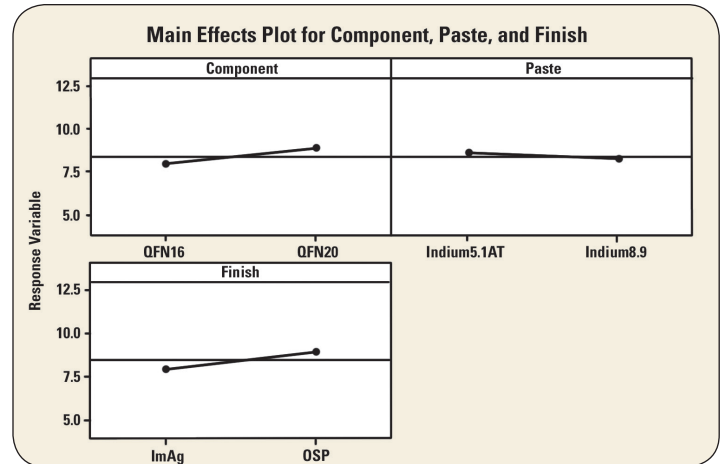


Figure 13. Main effects plot of insignificant factors.

These conclusions were very generic taking into consideration all factors and levels. Table 5 lists significant factors and interactions. Further conclusions were derived based upon the interaction plots and specific data sets that were identified as critical. The interaction plots, Figure 14 and Figure 15, reveal that for any given pattern and percentage, Tent-250 profile gave considerably less voiding. Figure 15 also shows that 30% solder paste print gave consistent results for both profiles.

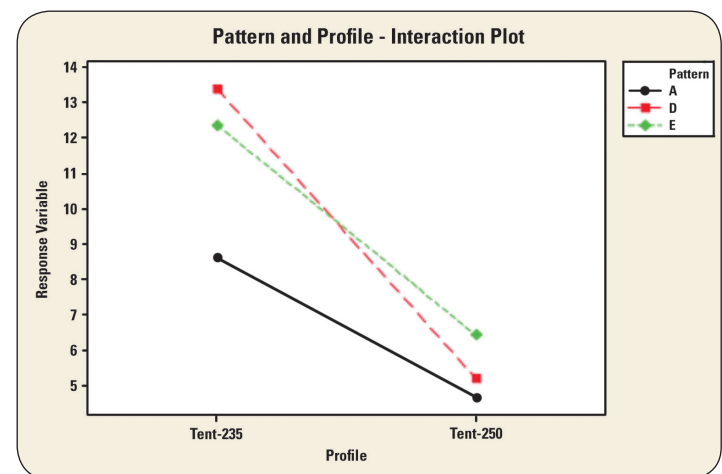


Figure 14. Interaction plot—pattern and profile.

Some of the insignificant factors, when combined with other significant factors, seem to influence the void formation. For example, the percentage and finish interaction plot (Figure 16) showed that OSP finish gave more voiding for 30% paste volume, when compared to ImAg finish. For 50% paste volume, OSP gave better results and for 70% both the finishes performed the same. This behavior can possibly be attributed to the flux content.

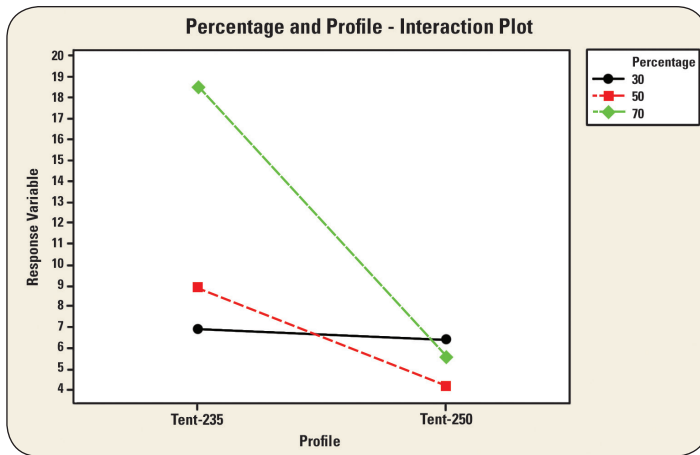


Figure 15. Interaction plot—percentage and profile.

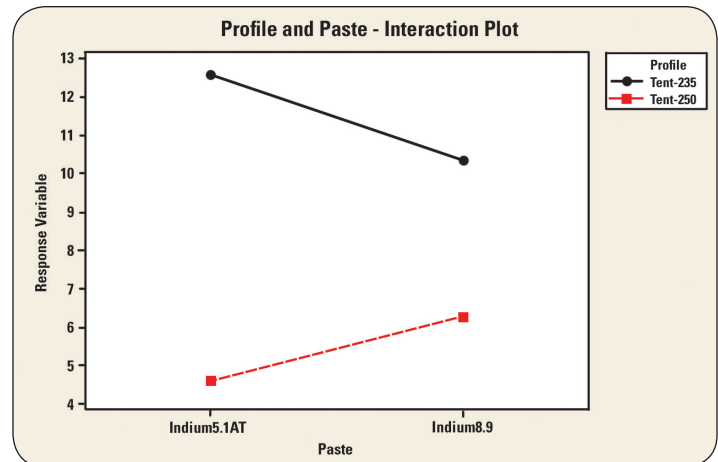


Figure 17. Interaction plot—profile and paste.

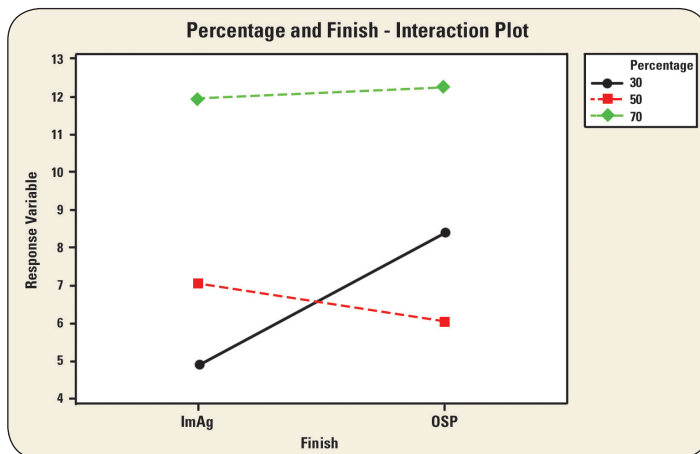


Figure 16. Interaction plot—percentage and finish.

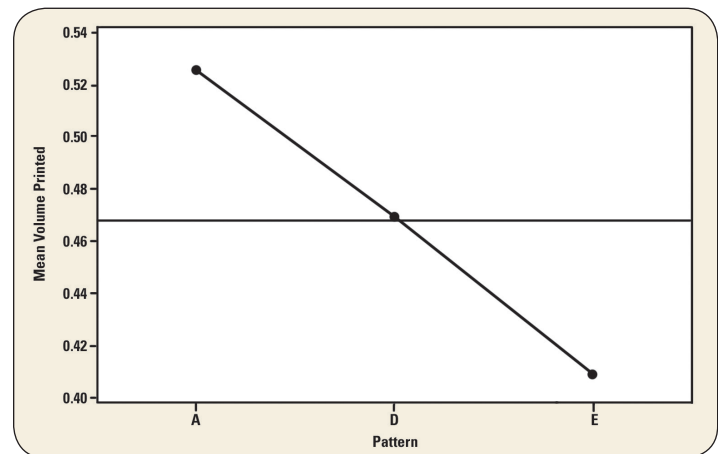


Figure 18. Pattern vs. mean volume printed.

OSP is more prone to contamination and hence requires aggressive fluxing to provide good wetting. Based on the graph, it can be concluded that 50% paste provided adequate fluxing for OSP finish, when compared to 30% paste. On the other hand, 70% paste volume had more flux which in turn resulted in excess voids.

The profile and paste interaction plot (Figure 17) revealed that when using Tent-235 profile, Indium8.9 Solder Paste performs better and when using Tent-250 profile, Indium5.1AT Solder Paste performs better.

The volume of the solder paste printed as a function of stencil aperture was also evaluated in this study. It was found that for any given paste percentage, the volume decreased from A to D and from D to E (Figure 18). The decrease in actual paste volume can possibly be attributed to the small aperture segments in the stencil, i.e., for any given paste percentage, the actual paste volume decreases as the number of openings in the stencil increases. The walls of the aperture played a predominant role in controlling the volume of the paste deposited.

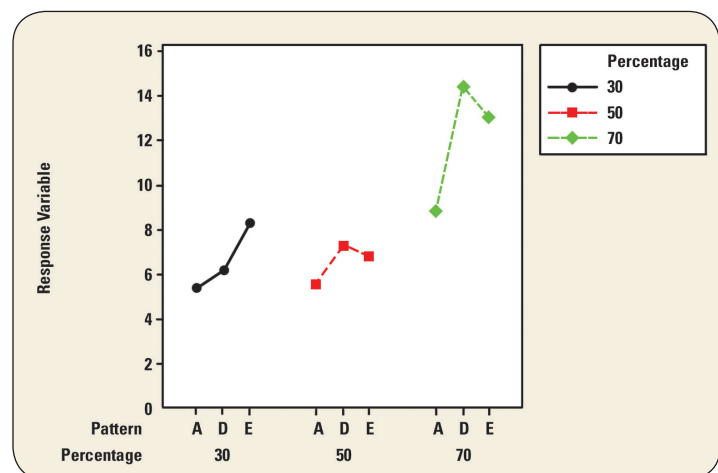


Figure 19. Percentage and pattern influence on void formation.

Figure 19 shows the influence of pattern and percentage on the void formation. Two important observations that were derived include the following: (1) for 30% paste, voids increased from pattern A to D and from pattern D to E, (2) for 50% and 70% paste volumes, there was a

decrease in void formation from pattern D to E. Even with all these pattern and percentage inferences it is still not clear as to the pattern and percentage combination that provides the least voids. Further analysis included in the following sections will attempt to identify specific favorable combinations for a given paste, profile, and finish.

Several significant factors were plotted against the aperture separation distance. These plots helped in understanding the impact of aperture geometry on the formation of voids. The box plots that follow (Figure 20–Figure 22) illustrate the relationship between paste, profile, finish, separation distance, and void formation. In the following box plots, the pattern and percentages were combined for better interpretation. A1, A2, and A3 indicates pattern A with 30%, 50%, and 70% paste volumes respectively. Therefore, combinations A1, D1, and E1 would theoretically have the same volume.

The following conclusions could be derived from the box plots:

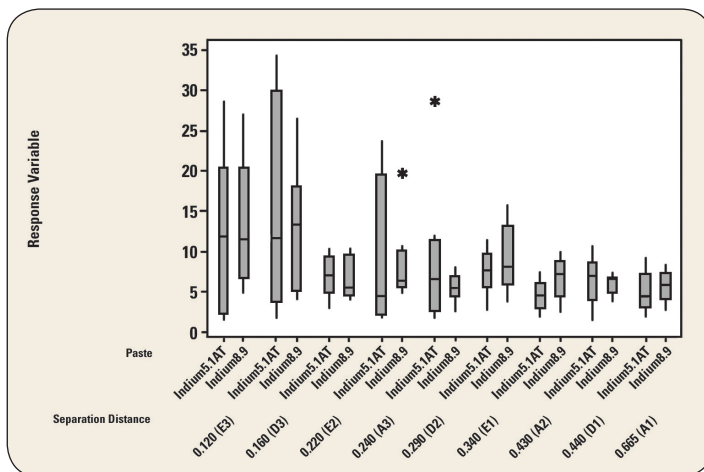


Figure 20. Box plot for paste and separation distance.

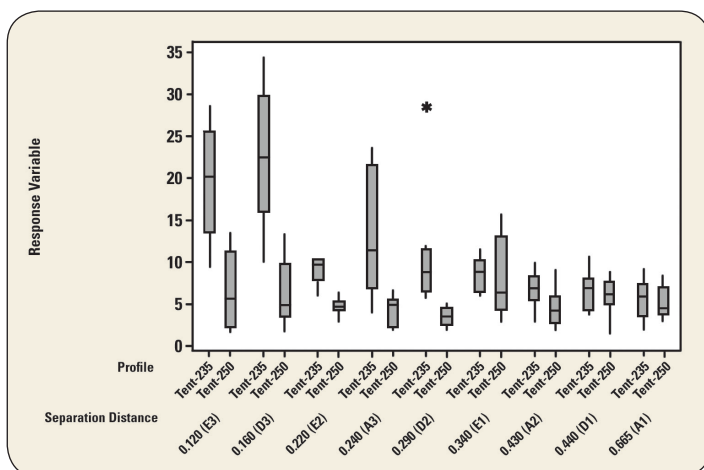


Figure 21. Box plot for profile and separation distance.

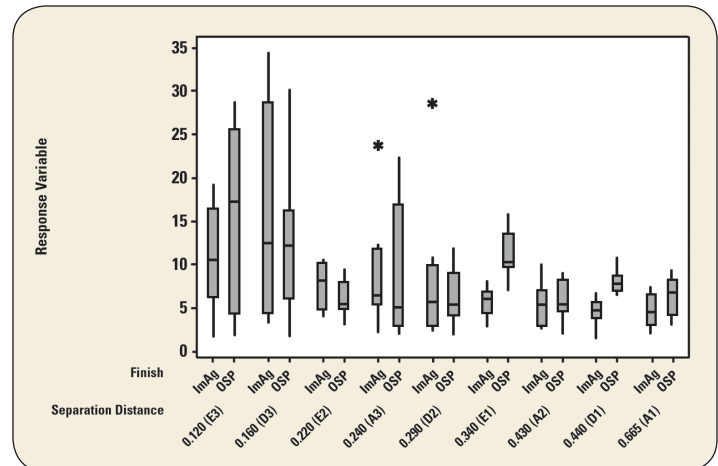


Figure 22. Box plot for finish and separation distance.

1. As the separation distance increased, both pastes, both profiles, and both finishes provided reduced amounts of voiding.
2. The lower the separation distance, the greater the spread in the data in all three plots. As the separation distance increased, the spread in the data decreased considerably.
3. When the separation distance was small, Tent-235 gave more voiding when compared to Tent-250. However, as the separation distance increased, the performance of both the pastes tended to get better and similar.

The effect of the separation distance on the void formation was one significant finding in our analysis.

Some of the key findings from the experimental study are:

1. For any given factor, the Tent-250 profile provided the least voids. Indium5.1AT Solder Paste performed better under the Tent-250 profile.
2. The ImAg finish performed largely better compared to OSP.
3. The thermal area of QFN16 had minimal voids when compared to QFN20.

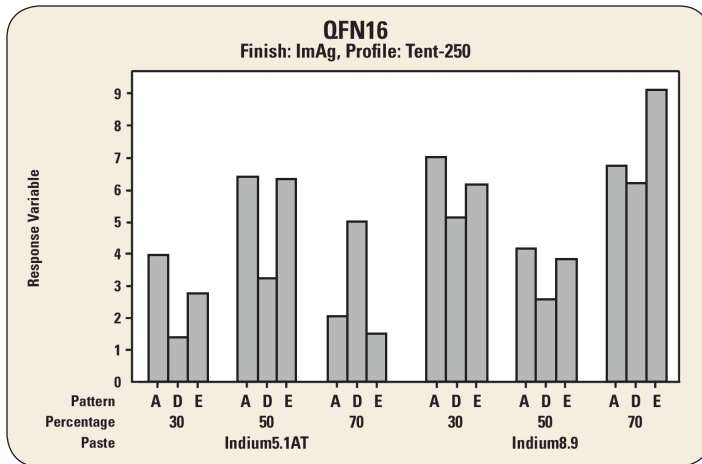


Figure 23. Plot of ImAg finish and Tent-250 profile—QFN16.

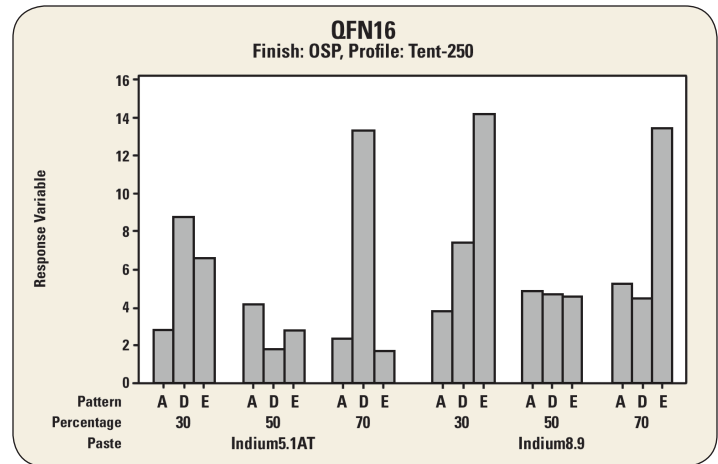


Figure 25. Plot of OSP finish and Tent-250 profile—QFN16.

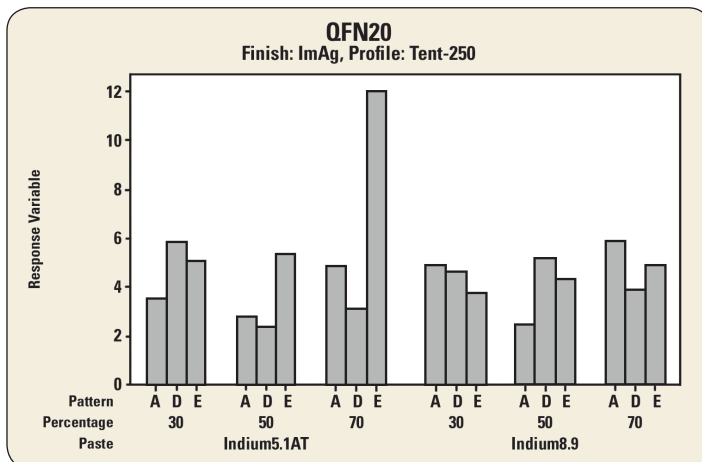


Figure 24. Plot of ImAg finish and Tent-250 profile—QFN20.

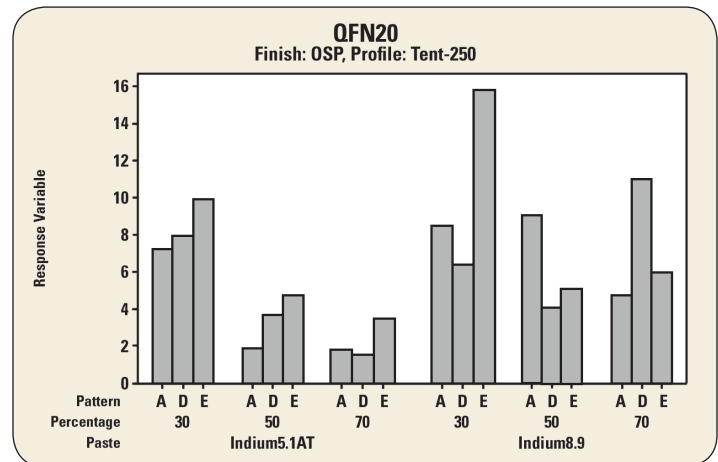


Figure 26. Plot of OSP finish and Tent-250 profile—QFN20.

Table 6. Summary of optimal patterns (ImAg finish and Tent-250).

Component	Percentage	Indium5.1AT	Indium8.9
QFN16	30	D	D
	50	D	D
	70	E	D
QFN20	30	A	E
	50	D	A
	70	D	D

The bar charts in Figures 23 and 24 were used to arrive at optimal paste percentages and patterns for ImAg finish and Tent-250 profile. Table 6 provides a summary of the patterns and percentages which provided least voids. It was observed that pastes which were printed using the modified stencil design provided least voiding. For QFN16 and Indium5.1AT Solder Paste, pattern E and 70% paste volume provided least voiding. Similarly for QFN16 and Indium8.9 Solder Paste, pattern D with 50% solder paste gave fewer voids.

Table 7. Summary of optimal patterns (IOSP and Tent-250).

Component	Percentage	Indium5.1AT	Indium8.9
QFN16	30	A	A
	50	D	E
	70	E	D
QFN20	30	A	D
	50	A	D
	70	D	A

Pattern D with 50% solder paste performed better for QFN20 and Indium5.1AT Solder Paste combinations. Similarly pattern A and 50% paste provided fewer voids for QFN20 and Indium8.9 Solder Paste combinations.

The bar charts in Figures 25 and 26 were used to arrive at optimal paste percentages and patterns for the OSP finish and Tent-250 profile. Table 7 provides a summary of the patterns and percentages which provided least voids for the OSP finish.

For the QFN16 and Indium5.1AT Solder Paste combination, pattern E with 70% paste yielded fewer voids. On the other hand, pattern A with 30% paste resulted in fewer voids for Indium8.9 Solder Paste. Similarly, for the QFN20 and Indium5.1AT Solder Paste combination, pattern D with 70% paste performed better. Pattern D with 50% paste resulted in fewer voids for Indium8.9 Solder Paste.

Conclusions

The experimental study helped us to identify a number of key findings which are listed below:

1. One significant finding that substantiated the literature review was breaking down the stencil aperture for the thermal pad in a series of smaller segments in order to minimize voids.
2. Aperture separation distance played a significant role in minimizing voids. Larger aperture separation distance provided more room for the volatiles to escape the solder during the reflow process.
3. The finish type played a significant role in the formation of voids. In our analysis, ImAg performed better when compared to OSP.
4. The influence of the component type on void formation was evident. QFN16 performed better than QFN20. The larger pitch size (0.8mm) allowed more chances for the volatiles to escape from inside the thermal area.
5. 30% paste volume gave less voiding, compared to 50% and 70% paste volume.
6. Void increase was directly proportional to the solder volume. For higher volumes (50% and 70%), voiding could be decreased using modified stencil apertures.
7. The influence of paste, when coupled with the reflow profile, became a significant factor. Overall both pastes performed better under the Tent-250 profile.
8. The reflow profile with 250°C peak temperature provided fewer voids under all circumstances.

Acknowledgements

The authors would like to acknowledge the generous support of Indium Corporation in carrying out this project. The authors are also grateful to Dr. Joseph G. Voelkel, Graduate Program Chair - The John D. Hromi Center for Quality and Applied statistics for his expert advice in analyzing the experiment. The authors also appreciate the efforts taken by Kasthuri Sankar Damodharan and Milan Shah for carrying out the experiments and preliminary analysis. The authors also extend their gratitude to the equipment donors for providing the Center for Electronics Manufacturing and Assembly (CEMA) with the required equipment for conducting training and applied research projects.

References

1. Ahmer Syed and WonJoon Kang, "Board Level Assembly and Reliability Considerations for QFN Type Packages," pp. 1-6.
2. Mark Kwoka and Jim Benson, "PCB Land Pattern Design and Surface Mount Guidelines For QFN Packages," pp. 2-6.
3. Joelle Arnold, Dr. Craig Hillman, Dr. Nathan Blattau and Jim McLeish "Design and Process Guidelines for QFNs: Manufacturability and Compatibility," pp. 2-7.
4. David Bernard and Bob Willis, "Common Process Defect Identification of QFN Packages Using Optical and X-ray Inspection."
5. Donghyun Ki, Mudasir Ahmad and Sue Teng, "Reliability Study of Lead-free SnAgCu Solder Joints Vs. SnPb Solder Joints in QFN Packages."
6. Krishnamoorthi, S.; Goh, K.Y.; Chong, D.Y.R.; Kapoor, R.; Sun, A.Y.S., "Thermal characterization of a thermally enhanced QFN package," pp. 485-490.
7. Tan Chee Eng; Fonseka, G, "QFN Miniaturization: Challenges and Solutions," pp. 314-319.
8. Tan Chee Eng; Pan Yen Jeat; Chin Meei Lian; Chin Lap Sin; Fonseka, G, "QFN assembly dilemma – solutions," pp. 1-5.
9. Montes de Oca, T.; Joiner, B.; Koschmieder, T "Impact of board variables on the thermal performance of a QFN package," pp. 512-519.
10. Sun, Wei; Zhu, W.H.; Danny, Retuta; Che, F.X.; Wang, C.K.; Sun, Anthony Y.S.; Tan, H.B, "Study on the Board-level SMT Assembly and Solder Joint Reliability of Different QFN Packages," pp. 1-6.
11. McCann, D.R.; SunHo Ha, "Package characterization and development of a flip chip QFN package: fcMLF," pp. 365-371.
12. Chai, T.C.; Quek, S.; Hnin, W.Y.; Wong, E.H.; Chia, J.; Wang, Y.Y.; Tan, Y.M.; Lim, C.T., "Board level drop test reliability of IC packages," Vol. I, pp. 630-636.

**First published at 2009 Electronic Components
and Technology Conference, May 26-29, 2009,
San Diego, California, USA.**